REMARKS

The following remarks are made in response to the Non-Final Office Action mailed July 7, 2006. Claims 1-34 were rejected. With this Response, claims 1 and 19 have been amended. Claims 1-34 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103

The Examiner rejected claims 1, 2, 6, 7, 9-13, 16, 17, 19, 20, 23-29, 32, and 33 under 35 U.S.C. § 102(e) as being anticipated by the Futral et al. U.S. Patent No. 5,991,797.

The Examiner rejected claims 3-5, 8, 21, 22, and 25 under 35 U.S.C. § 103(a) as being unpatentable over the Futral et al. U.S. Patent No. 5,991,797 in view of the Regnier et al. U.S. Patent No. 6,647,423.

The Examiner rejected claims 14, 15, 18, 30, 31, and 34 under 35 U.S.C. § 103(a) as being unpatentable over the Futral et al. U.S. Patent No. 5,991,797 in view of the Forin et al. U.S. Patent No. 6,360,220.

Amended independent claim 1 claims a method of managing memory in a distributed computer system and amended independent claim 19 claims a distributed computer system. Amended independent claim 1 and amended independent claim 19 include limitations related to binding a remote key to a first address representing a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode including a first processor and the first memory; sending the bound remote key and first address from the first host processor endnode to a second host processor endnode on a communication fabric via a first network interface controller (NIC) in the first host processor endnode and a second NIC in the second host processor endnode, wherein the second host processor endnode includes a second processor and a second memory; and performing a remote direct memory access operation from the second host processor endnode with a second consumer process stored in the second memory to access the contiguous memory address range including sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC. The Futral et al. patent does not teach or suggest all of these limitations.

The Futral et al. patent teaches a method for directing transfer of input/output (I/O) of an I/O device to other processing units in a computer system including first and second processing units and an I/O unit coupled to an interconnect fabric. The second processing unit controls access to the I/O unit, which is coupled to an I/O device. Memory fragments of the first processing unit are registered with the interconnect fabric to get memory handles for the memory fragments. A list is created having an identifier of the first processing unit, the memory handles, and virtual addresses and links of memory fragments. The list is sent from the first processing unit to the second processing unit. The list is sent from the second processing unit to the I/O unit. The identifier of the first processing unit is examined and a communications connection from the I/O unit to the first processing unit is determined. I/O data is transferred over the communication connection between and I/O unit and memory referenced by the memory handles and virtual addresses. The method supports peer-to-peer operation where a number of different I/O units, each with its own physical memory addressing domain, require access to the same I/O device. In the embodiment specifically described at column 5 referenced by the Examiner, the combination of a platform identifier, a memory handle for registered memory, and a virtual address uniquely identifies memory located anywhere in a clustered computer system.

Thus, the Futral et al. patent does not teach or suggest limitations of amended independent claim 1 and amended independent claim 19 related to performing **a remote direct memory access operation from a second host processor endnode with a second consumer process stored in a second memory of the second host processor endnode** to access a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode, wherein the remote direct memory access operation includes sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC. Instead, the Futral et al. patent teaches a second host system directing **an I/O device to transfer data between** a requesting application program's buffers on **a first host system and an I/O unit** coupled to the I/O device **without the need to pass through the second host system**, where the second host system retains control of the I/O request.

In the Examiner's response to Applicants' arguments, the Examiner equates "I/O device" or "I/O unit" or "host" as interchangeable terms. These terms and their definitions in the method and computer system disclosed in the Futral et al. patent are all distinctly defined as summarized in the above remarks. Accordingly, a host processor endnode in amended independent claims 1 and 19 and as clearly defined in the current specification is in no way equivalent to an I/O device or I/O unit. This distinction is clear from both the current specification and claims and the disclosed method and computer system of the Futral et al. patent.

In addition, the Examiner states in the response to Applicants' arguments that the "SAN NIC" inherently contains a processor and memory. As clarified, both amended independent claim 1 and amended independent claim 19 specifically define operations performed by a first network interface controller (NIC) in the first host processor endnode and a second NIC in the second host processor endnode. The Futral et al. patent also specifically defines functions of the SAN NICs in its described computer system. Thus, it is clear, in amended independent claims 1 and 19 the first processor and the first memory in the first host processor endnode are separate and distinct from the NIC in the first processor endnode and the second processor and the second memory in the second host processor endnode are separate and distinct from the second NIC in the second host processor endnode.

In view of the above, the Futral et al. patent does not teach or suggest the method of amended independent claim 1 or the distributed computer system of amended independent claim 19. Furthermore, dependent claims 2-18 further define patentable distinct amended independent claim 1 and dependent claims 20-34 further define patentably distinct amended independent claim 19. Therefore, these dependent claims are also believed to be allowable.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102 and § 103 rejections to claims 1-34, and requests allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-34 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-34 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or Kevin Hart at Telephone No. (970) 898-7057, Facsimile No. (970) 898-7247. In addition, all correspondence should continue to be directed to the following address:

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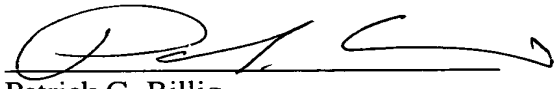

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 7 day of December, 2006.

By: 
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